CLAIMS

What is claimed is:

1. A method of fabricating an interposer substrate for attaching to an active surface of a semiconductor die having a plurality of conductive bumps protruding transversely therefrom, the method comprising:

providing a substrate having a first surface and a second surface, said substrate including a dielectric layer and a plurality of conductive elements on said dielectric layer adjacent said second surface; and

forming a plurality of recesses in said first surface of said substrate and through said dielectric layer to a depth through said dielectric layer to expose at least a portion of a contiguous conductive element adjacent said second surface and of a size and configuration to receive said plurality of conductive bumps of said semiconductor die so that said plurality of conductive bumps is substantially received within said plurality of recesses.

2. The method of claim 1, wherein said forming said plurality of recesses comprises forming said plurality of recesses to a depth so that a surface of each of said plurality of conductive bumps will contact at least a portion of a said contiguous conductive element with said active surface of said semiconductor die abutting said first surface of said substrate.

3. The method of claim 1, further comprising forming at least one opening in said second surface of said substrate in communication with at least one recess of said plurality.

4. The method of claim 1, wherein said providing said substrate comprises forming said plurality of conductive elements by at least one of printing conductive ink and etching a conductive layer.

5. The method of claim 1, wherein said providing said substrate comprises disposing a solder mask over said plurality of conductive elements in a pattern leaving portions of said plurality of conductive elements exposed.

6. The method of claim 1, wherein said providing comprises providing said dielectric layer as a flexible polymer material.

7. The method of claim 1, wherein said providing comprises providing said substrate to include at least one of BT, FR4 laminate, FR5 laminate and UPILEX®.

8. The method of claim 1, wherein said forming said plurality of recesses comprises collectively configuring said recesses in a centrally aligned row in said substrate to correspond with a conductive bump configuration on said semiconductor die.

9. The method of claim 1, wherein said forming said plurality of recesses comprises collectively configuring said recesses in a peripheral configuration in said substrate to correspond with a conductive bump configuration on said semiconductor die.

10. The method of claim 1, wherein said forming said plurality of recesses comprises collectively configuring said recesses in an I-shaped configuration in said substrate to correspond with a bump configuration on said semiconductor die.

11. The method of claim 1, wherein said forming said plurality of recesses comprises forming said plurality of recesses by at least one of a wet etch, dry etch, mechanical drilling, mechanical punching and laser ablation.

12. The method of claim 1, wherein said forming said plurality of recesses comprises patterning said plurality of recesses, each substantially with a peripheral shape including at least one of a square, rectangle, circle and oval.

13. The method of claim 1, wherein said forming said plurality of recesses comprises forming at least one sloped side wall in each of said plurality of recesses.

14. The method of claim 1, wherein said forming said plurality of recesses comprises forming at least one side wall in each of said plurality of recesses to be substantially normal with said first surface of said substrate.